5. (Amended) A signal processing circuit according to Claim 1, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

6. (Amended) A signal processing circuit according to Claim 1, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

7. (Amended) A signal processing circuit according to Claim 1, wherein said first input-output circuit is a video input-output circuit that receives or transmits video data, said dedicated processing circuit is a video processing circuit including at least one of an encoding circuit, a decoding circuit, a discrete cosine transform circuit, an inverse discrete cosine transform circuit, a motion estimation circuit, and a motion compensation circuit.

8. (Amended) A signal processing circuit according to Claim 7, wherein said memory access control circuit includes a control means that stores image data received in real-time in said local memory by way of said first input-output circuit, said second local bus, and said third connection circuit, and that transfers the image data stored in said local memory to said video processing circuit by way of said second connection circuit and said first local bus.

9. (Amended) A signal processing circuit according to Claim 7, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

a1

10. (Amended) A signal processing circuit according to Claim 7, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.

Please add the following new claims:

11. (Added) A signal processing circuit according to Claim 2, further comprising a second input-output circuit that is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

12. (Added) A signal processing circuit according to Claim 2, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.

a2

13. (Added) A signal processing circuit according to Claim 3, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.

14. (Added) A signal processing circuit according to Claim 11, further comprising a third input-output circuit that receives or transmits a serial signal, produces an interrupt request

to be issued to said microprocessor, and transfers the serial signal over said system bus under control of said microprocessor.

15. (Added) A signal processing circuit according to Claim 2, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

16. (Added) A signal processing circuit according to Claim 3, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

17. (Added) A signal processing circuit according to Claim 11, further comprising a timer that cyclically applies an interrupt signal to said microprocessor, and a control means that includes a status register which indicates the processing state of said dedicated processing circuit, and an instruction register in which said microprocessor sets processing to be performed by said dedicated processing circuit, wherein:

said microprocessor reads a value from said status register in response to the cyclic interrupt signal, and judges whether the next processing instruction can be issued to said dedicated processing circuit; and

when the next processing instruction can be issued, said control means allows the instruction to be written in said instruction register.

18. (Added) A signal processing circuit according to Claim 2, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

19. (Added) A signal processing circuit according to Claim 3, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

20. (Added) A signal processing circuit according to Claim 11, wherein data that should be processed by said dedicated processing circuit is stored in said local memory, and data stored in said local memory is read by way of said third connection circuit, said second local bus, and said input-output circuit.

21. (Added) A signal processing circuit according to Claim 2, wherein said first input-output circuit is a video input-output circuit that receives or transmits video data, said dedicated processing circuit is a video processing circuit including at least one of an encoding circuit, a decoding circuit, a discrete cosine transform circuit, an inverse discrete cosine transform circuit, a motion estimation circuit, and a motion compensation circuit.

22. (Added) A signal processing circuit according to Claim 21, wherein said memory access control circuit includes a control means that stores image data received in real-time in said local memory by way of said first input-output circuit, said second local bus, and

said third connection circuit, and that transfers the image data stored in said local memory to said video processing circuit by way of said second connection circuit and said first local bus.

23. (Added) A signal processing circuit according to Claim 21, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

24. (Added) A signal processing circuit according to Claim 8, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

25. (Added) A signal processing circuit according to Claim 22, further comprising a second input-output circuit that receives or transmits a voice signal, is connected to said system bus, produces an interrupt request to be issued to said microprocessor, and transfers data over said system bus under control of said microprocessor.

26. (Added) A signal processing circuit according to Claim 21, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.

27. (Added) A signal processing circuit according to Claim 8, further comprising a third input-output circuit that receives or transmits a serial signal that is either an encoded video signal or an encoded voice signal, produces an interrupt request to be issued to said microprocessor, and transfers data of the serial signal over said system bus under control of said microprocessor.